

Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

Sub  
B1

1. (Currently amended) A method of providing a plurality of emulation instructions to a processor from an emulation instruction register, the method comprising:

receiving a plurality of emulation instructions simultaneously from the emulation instruction register;  
determining a the validity of a first emulation instruction of the plurality of emulation instructions by reading width bits in the first emulation instruction;

providing the first emulation instruction of the plurality of instructions to a decoder of the processor if the first emulation instruction is valid;

determining a the validity of a second emulation instruction of the plurality of emulation instructions by reading width bits in the second emulation instruction; and

providing the second emulation instruction of the plurality of instructions to the decoder if the second emulation instruction is valid.

*(A)* B) 2. (Currently amended) The method of Claim 1, further comprising determining a ~~the~~ size of the plurality of emulation instructions.

3. (Currently amended) The method of Claim 1, further comprising storing the plurality of emulation instructions in the a-single emulation instruction register in subsequent clock cycles.

4. (Currently amended) The method of Claim 1, further comprising receiving loading the second emulation instruction ~~of~~ ~~the plurality of instructions~~ after determining the first emulation instruction is invalid.

5. (Currently amended) The method of Claim 1, further comprising loading the plurality of emulation instructions in parallel into the emulation instruction register.

6. (Currently amended) The method of Claim 1, further comprising providing the second emulation instruction to the decoder after the first emulation instruction is completed.

7. (Currently amended) The method of Claim 1, further comprising providing the plurality of emulation instructions to the decoder after a first run-test idle state without receiving multiple RTIs entering into a second run-test idle state.

8. (Currently amended) The method of Claim 1, further comprising providing the first and second emulation instructions to a digital signal processor.

9. (Currently amended) A method of providing processing instructions to within a processor, the method comprising:  
loading a plurality of instructions into an a single instruction register;  
receiving an RTI a run-test idle state signal;  
simultaneously providing the plurality of instructions to the processor; and  
processing the plurality of instructions without receiving another run-test idle state signal.

10. (Currently amended) The method of Claim 9, further comprising loading the plurality of instructions instruction into an N-bit emulation instruction register.

*(X) 8 B1*  
11. (Currently amended) The method of Claim 9, further comprising determining a ~~the~~ validity of each of the plurality of instructions before processing by reading bits in each instruction indicating a width of the instruction.

12. (Currently amended) The method of Claim 11, further comprising aborting ~~the~~ processing of any invalid instructions and loading a next instruction of the plurality of instructions from the instruction register.

13. (Currently amended) The method of Claim 9, further comprising loading a next instruction of the plurality of instructions from the instruction register if a no-operation instruction is loaded.

14. (Currently amended) The method of Claim 9, further comprising providing the plurality of instructions ~~instruction~~ to the processor a plurality of times without reloading the instruction register.

15. (Original) The method of Claim 9, further comprising providing the plurality of instructions to a digital signal processor.

*AS B*

16. (Currently amended) A processor comprising:  
an instruction register adapted to store a plurality of  
emulation instructions;  
emulation control logic adapted to control a the flow of  
the plurality of emulation instructions to a processor pipeline  
following detection of a single run-test idle state RTI; and  
a decoder to which may receive the plurality of  
instructions for processing.

17. (Canceled)

18. (Currently amended) The processor of Claim 16,  
wherein the emulation control logic determines a the validity of  
the plurality of instructions by reading bits in each  
instruction indicating a width of each instruction and discards  
any invalid instructions.

19. (Currently amended) The processor of Claim 16,  
wherein the emulation control logic loads a next instruction  
from the instruction register immediately after detecting a no-  
operation instruction.

*ASB*  
20. (Currently amended) The processor of Claim 16,  
wherein the processor is a digital signal processor.

21. (Currently amended) An apparatus, including operating  
instructions residing on a machine-readable storage medium, for  
use in a device machine system to handle a plurality of  
emulation instructions, the operating instructions causing the  
device machine to:

load the plurality of emulation instructions into a single  
emulation instruction register;

enter a receive and run-test idle state RTI;

provide the plurality of emulation instructions to a the  
processor; and

process the plurality of emulation instructions.

22. (Canceled)

23. (Currently amended) The apparatus of Claim 21,  
wherein a the validity of each of the plurality of emulation  
instructions is determined before processing by reading bits in  
each emulation instruction indicating a width of each emulation  
instruction.

*AB*

24. (New) The method of Claim 1, further comprising:  
scanning emulation instructions from an in-circuit emulator  
(ICE) to a Joint Test Action Group (JTAG) interface; and  
loading emulation instructions from the JTAG interface to  
the emulation instruction register.

25. (New) The method of Claim 1, wherein a pre-determined  
set of width bits indicates an instruction is invalid.

26. (New) The processor of Claim 16, wherein the  
instruction register comprises first and second registers.

27. (New) The processor of Claim 16, wherein the emulation  
control logic comprises a state machine.

28. (New) The processor of Claim 16, further comprises a  
multiplexer to select between an emulation instruction for the  
plurality of emulation instructions to send to the processor  
pipeline.

29. (New) The apparatus of Claim 21, further comprising an  
in-circuit emulator to monitor operations of the processor.

~~13~~  
30. (New) The method of Claim 1, further comprising  
executing at least one of the plurality of emulation  
instructions to monitor operation of the processor.